## REMARKS

This communication is responsive to the Office Action mailed January 17, 2003. Claims 1-21 remain pending in the application. Minor amendments are made to the specification to correct typographical errors. No new matter is added by these amendments.

**Section 102 Rejections**

All claims stand rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 5,748,551, issued May 5, 1998, ("Ryan"), which is owned by the assignee of the present invention.

Applicant respectfully submits that the Ryan reference fails to disclose each and every element of the independent claims of the present application. Applicant emphasizes that independent claims 1, 5, and 19 of the present invention each require the element of "a supplementary command bus." Ryan, however, does not disclose the element of a supplementary command bus. Ryan only discloses a single command bus.

The Examiner states that Ryan discloses "a supplementary command bus (ABSTRACT) for transferring a second command, wherein the second command does not relate to the first memory location (ABSTRACT, Column 9, lines 5-50)." Applicant respectfully disagrees. In fact, the Abstract of the invention never mentions a dual command bus system, or any functionality that would imply the existence of a main and a supplementary command bus.

Only a single command bus is identified throughout the Ryan reference, and thus, no differentiation is made between main and supplementary command busses nor the functions they may perform. The abstract of Ryan states that, "[c]ommands and addresses applied to

the memory device affect all internal banks identically, but on a time staggered basis." Such commands are performed on a time-staggered basis because only one command can be sent on the command bus at a time. In contrast, in the present invention, both a main command bus and a supplementary command bus may be used in parallel such that location specific commands and overall commands can be processed at the same time. For example, a location specific ACTIVATE command may be transmitted to bank 1 at the same time a PRECHARGE command may be transmitted (on the supplemental command bus) is transmitted to all addresses on bank 0.

The Examiner further states that Ryan discloses a supplementary command bus that transfers only general commands, at Column 7, lines 21-63, and main and supplementary control interfaces, at Figure 7, 202, 203, and Column 6, lines 5-67. Applicant respectfully disagrees. These referenced portions of the patent, and all other parts of the Ryan patent, fail to disclose a supplementary command bus. Rather, Figure 7 and the referenced text clearly only discuss and illustrate a single command bus and a related address bus. The address bus does not carry commands and is not a supplementary command bus.

Indeed, it is not surprising that Ryan does not disclose a supplementary command bus element because the Ryan patent is directed towards an entirely different issue than the present application. One objective of the Ryan reference is to reduce the idle time on a memory device bus. This is done by using multiple banks and therefore reducing the possibility of having to wait between accessing different rows. In contrast, the present application is directed towards increasing bandwidth to the memory device. See, e.g., paragraph 4 of the present application describing the problem to be overcome, "[c]ertain access processes saturate the command/address bus, limiting the throughput/bandwidth of the

memory device." By off-loading non-location specific commands to a supplemental bus, more commands can be carried on the main command bus.

Similarly, independent claims 8 and 11 of the present invention require the element of "a general command interface" configured to receive a general command. Also, independent claim 16 requires the element of "a supplementary control interface for receiving a general command." The remarks relevant to claims 1, 5, and 19 are similarly applicable to claims 8, 11, and 16. The general command is associated with commands "that are not associated with row or column information, and thus do not utilize the address bus." See, *e.g.*, page 7, paragraph 26 of the present application. The general command of claim 8 is fundamentally different from the "location-specific command interface" of claim 8, and the memory interface is configured with separate input interfaces for each type of command.

Claim 14 requires "a one-bit PRECHARGE input dedicated to receiving a PRECHARGE command." Ryan does not disclose a dedicated one-bit PRECHARGE input. Any PRECHARGE input received by the memory of the Ryan patent is also configured to receive many other types of commands, including location specific commands.

Finally, Claim 20 recites a method including the step of in a third time slot, requesting activation of a second row and requesting closure of the first row. Ryan does not disclose a method of accessing memory wherein, during a single time slot, activation of a second row and closure of a first row can be performed simultaneously.

**B. Conclusion**

Applicant respectfully submits that the present application is in condition for allowance, and earnestly solicits a Notice of Allowance at the Examiner's earliest

convenience. The Examiner is invited to telephone the undersigned if such would advance prosecution of this Application in any way.

Dated this 20th day of March, 2003.

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